Flow of Instructions

* IMME
  + PC -> Instruction Memory.
  + Instruction Memory -> Decoder. Instruction Memory -> ImmeLUT
  + ImmeLUT -> RegFile
* Branch
  + PC -> Instruction Memory.
  + Instruction Memory -> Decoder. Instruction Memory -> branchLUT
  + branchLUT -> PC
* R-type
  + PC -> Instruction Memory.
  + Instruction Memory -> Decoder. Instruction Memory -> RegFile
  + RegFile -> ALU
  + ALU -> RegFile
* LW & SW
  + PC -> Instruction Memory.
  + Instruction Memory -> Decoder. Instruction Memory -> MemAddressLUT Instruction Memory -> RegFile
  + MemAdressLUT and RegFile -> Memory.
  + Memory -> RegFile.

Components (Single Cycle)

* PC
  + Basic PC, just take in an address and write it into PC
  + PC is always written into.
* Instruction Memory
  + Basic LUT pre-loaded with instructions, give address get instructions
* Decoder
* RegFile
  + Always read out RS and RT. Have 2 lines of data in: 1 for RS, 1 for COUT. 2 Flags, 1 for RS, 1 for COUT.
  + Inputs:
    - 2 bits RS address
    - 3 bits RT address
    - COUT write only to dedicated COUT registers
* ALU
  + Pure Combinational logic, 2 inputs 1 output. 1 flag to specify which operation.
* Memory
  + 1 Line for Data, 1 Line for address. 2 flags to specify whether write or read is on. 1 Output for requested data if read is on.
* LUT branch
  + Basic LUT pre-loaded with target branch address
* LUT Immediate
  + Basic LUT pre-loaded with immediates
* LUT MemoryAddress
  + Basic LUT pre-loaded with Memory Addresses for LW and SW.